WHAT IS CLAIMED IS:

1. A circuit, comprising:

a hardware-based adaptive differential pulse code modulation (ADPCM) decoder;

a memory storing both programming instructions and ADPCM encoded source file data; and

a micro-controller having an architecture that implements time multiplexed memory addressing wherein ADPCM encoded source file data is extracted from the memory and delivered to the ADPCM decoder for processing in a first cycle, and wherein programming instructions are extracted from the memory and executed by the micro-controller in a second cycle while the hardware-based ADPCM decoder continues processing of the previously extracted ADPCM encoded source file data.

2. The circuit of claim 1 wherein the hardware-based ADPCM decoder operates to synthesize decoded output data from the extracted ADPCM encoded source file data without any processing assistance from the micro-controller.

3. The circuit of claim 2 wherein the decoded output data comprises linear pulse code modulation (PCM) format data.

4. The circuit of claim 1 wherein the architecture of the micro-controller comprises:

a program counter that supplies a memory address for retrieving micro-controller programming instructions;

an address counter that supplies a memory address for retrieving a portion of the ADPCM encoded source file data; and

a multiplexer connected to the program counter and the address counter and operating to select between program counter and address counter supplied memory addresses.

5. The circuit of claim 4 wherein the selection operation of the multiplexer is driven by a two phase clock signal having a first phase for selecting the address counter and a second phase for selecting the program counter.

6. The circuit of claim 4 wherein the architecture of the micro-controller further comprises:

a register storing an ending memory address for the ADPCM encoded source file data; and

a comparator for comparing the address counter supplied memory address to the register ending memory address and outputting an end signal when the compared addresses match.

7. The circuit of claim 6 wherein the architecture of the micro-controller further comprises:

means for incrementing the address counter to select over a plurality of first cycles the memory addresses necessary for retrieving all portions of the ADPCM encoded source file data for decoding.

8. The circuit of claim 1 wherein the first and second cycles consecutively repeat until all ADPCM encoded source file data is extracted for decoder processing.

9. The circuit of claim 1 wherein the memory comprises a read only memory (ROM).

10. The circuit of claim 1 wherein the circuit is fully implemented on an integrated circuit chip.

11. A method for time multiplexed addressing of a memory storing both programming instructions and adaptive differential pulse code modulation (ADPCM) encoded source file data, comprising the steps of:

extracting ADPCM encoded source file data from the memory for delivery to, and processing by, an ADPCM decoder in a first time cycle; and

extracting programming instructions from the memory for execution by a processor in a second time cycle while the ADPCM decoder continues processing of the first time cycle extracted ADPCM encoded source file data.

12. The method as in claim 11 wherein the step of extracting ADPCM encoded source file data comprises the step of selecting an address in the memory where a portion of the ADPCM encoded source file data is stored.

13. The method as in claim 12 wherein the step of extracting programming instructions comprises the step of selecting an address in the memory where each programming instruction is stored.

14. The method as in claim 13 further including the step of alternately choosing between the selected ADPCM encoded source file data address and the selected programming instruction address.

15. A programming architecture for a micro-controller connected to a memory storing both programming instructions and adaptive differential pulse code modulation (ADPCM) encoded source file data, the architecture comprising:

a program counter storing a first memory address relating to a micro-controller programming instruction;

an address counter storing a second memory address relating to a portion of the ADPCM encoded source file data;

a multiplexer receiving the first and second memory addresses and operating to select the first memory address for application to the memory during a first cycle and operate to select the second memory address for application to the memory during a second cycle.

16. The programming architecture of claim 15 further comprising a clock signal having a first and second phase to drive operation of the multiplexer selection between the first and second memory addresses, respectively.

17. The programming architecture of claim 15 further including:

a register storing a third memory address relating to a last portion of the ADPCM encoded source file data; and

a comparator operating to compare the first memory address to the third memory address and output a signal indicative of reaching an end of the ADPCM encoded source file data when the addresses match.

18. The programming architecture of claim 15 further including an instruction register operating to supply the first memory address relating to a micro-controller programming instruction to the program counter and supply the second memory address relating to a portion of the ADPCM encoded source file data to the address counter.

19. The programming architecture of claim 15 further including a first increment signal applied to the address counter to increment the second memory address during the second cycle to consecutively access all portions of the ADPCM encoded source file data.

20. The programming architecture of claim 19 further including a second increment signal applied to the program counter to increment the first memory address during the first cycle to change the micro-controller programming instruction.

21. An integrated circuit chip, comprising:

an adaptive differential pulse code modulation (ADPCM) decoder portion receiving ADPCM encoded source file data for decoding and outputting linear pulse code modulation (PCM) data;

a read only memory (ROM) portion storing both programming instructions and ADPCM encoded source file data; and

a micro-controller portion with a time multiplexed memory addressing architecture driven by a clock signal having a first phase and a second phase wherein a first address is applied to the ROM portion to extract ADPCM encoded source file data for delivered by the micro-controller portion to the ADPCM decoder for processing during the first phase, and wherein a second address is applied to the ROM portion to extract programming instructions for execution by the micro-controller during the second phase.

22. The chip of claim 21 wherein the ADPCM decoder operates to synthesize the linear PCM data from the

extracted ADPCM encoded source file data without any processing assistance from the micro-controller portion.

23. The chip of claim 21 wherein the ADPCM decoder portion operates to decode the first phase extracted ADPCM encoded source file data during the second phase micro-controller portion execution of programming instructions.

24. The chip of claim 21 wherein the architecture of the micro-controller portion comprises:

an address counter that supplies the first address for extracting ADPCM encoded source file data;

a program counter that supplies the second address for extracting micro-controller programming instructions; and

a multiplexer connected to the program counter and the address counter and operating responsive to the clock signal to select between address counter and program counter supplied memory addresses.

25. The chip of claim 24 wherein the architecture of the micro-controller further comprises:

a register storing an ending memory address for the ADPCM encoded source file data; and

a comparator for comparing the address counter supplied first address to the register ending memory address and outputting a signal when the compared addresses match indicative of reaching the end of extracting the ADPCM encoded source file data.

26. The chip of claim 25 wherein the architecture of the micro-controller portion further comprises:

a first increment signal applied to the address counter to increment the first address during the first phase of the clock signal to consecutively access all addresses of the ADPCM encoded source file data.

27. The chip of claim 26 wherein the architecture of the micro-controller portion further comprises:

a second increment signal applied to the program counter to increment the second memory address during the second phase of the clock signal to change the micro-controller programming instruction.